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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,982	07/30/2001	Michael John Erickson	10017845-1	9738

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EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/917,982	Applicant(s) ERICKSON ET AL.	
	Examiner Ted T. Vo	Art Unit 2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the communication filed on 7/30/2001.

Claims 1-20 are pending in the application.

Specification

2. It would require filling the blanks in paragraph [0001], page 1.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Deegan et al., (US no. 6,055,632).

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per claim 1:

Deegan states that firmware is an image stored in non-volatile memory of a processor module. Periodically, it is necessary or desirable to upgrade this firmware in order to improve the performance of the programmable controller system (see column 1, lines 25-29).

Deegan discloses a first computer/firmware provider (Claim limitation: 'firmware server') that stores a firmware image (see Fig. 1, reference character 40). A Motherboard (Claim limitation: 'Printed circuit board') that is

included with programmable part (integration) such as a non-volatile memory (see Fig. 1, reference character no. 24, 'NVM'). The motherboard is characterized to receive the firmware image downloading from the firmware provider via a network interface (see Fig. 1, reference character no. 38, "ETHERNET INTERFACE', reference character no. 30 'DAUGHTER BOARD'; and reference character no. 20 'MOTHERBOARD').

Deegan's teaching covers the claim limitation:

"***A method of implementing firmware updates to a programmable part within a circuit board, comprising the steps of:***

creating an image file of firmware (column 1, lines 25-29: it defines firmware image) ***used to program the part; storing the image file at a firmware server"*** (see column 3, lines 18-29, referring to: 'transferring a firmware update over a network' [This citation shows that the firmware is originally created and stored at a remote computer 'firmware provider' in the network]);

"integrating the programmable part (see Fig. 1, reference character no. 24, 'NVM' : ['NVM' stands for Non-Volatile Memory, a programmable device]) ***with the printed circuit board"*** (see Fig. 1, reference character no. 20 'MOTHERBOARD' [Mother board is a printed circuit board])***; and***

"networking with the firmware server such that the image file downloads to the circuit board for programming the programmable part" (see Fig. 1, reference character no. 51 'ETHERNET'; and see column 3, lines 52-65, referring to: 'network link, firmware upgrade can be downloaded into a processor module of a programmable controller system from a firmware provider" (Processor module according to citation is the Motherboard : see column 5, lines 25-26))***.***

As per claim 2: Deegan discloses, "***The method of claim 1, further comprising the step of automatically polling the firmware server to download the firmware to the circuit board***" (see column 5, lines 55-64, 'The Ethernet interface 38 also connects the programmable controller 10 with other programmable controller systems and permits messages to be sent back and forth between them' [polling], see column 6, lines 7-14, referring to: 'the processor 20 can be upgraded immediately after the user request an upgrade' [download the firmware to the circuit board]).

As per claim 3: Deegan discloses, "***The method of claim 1, further comprising the step of integrating a serial chip*** (see 'Ethernet interface 38', 'RAM 36', 'Dual port RAM 37' in Fig.1, or the combination of chips in DAUGHTER BOARD and MOTHERBOARD [Examiner note: The interpretation for serial chip is in accordance to the specification, wherein the specification at paragraph [0025], page 6, it refers to 'a serial or a memory device 26']) ***with the printed circuit board*** (reference character 20, 'MOTHERBOARD'), ***the serial chip polling the firmware server to download the firmware*** (see column 5, lines 55-64, 'The Ethernet interface 38 also connects the programmable controller 10 with other programmable controller systems and permits messages to be sent back and forth between them' [polling]), ***the programmable part having bootstrap software*** (see Fig. 2, referring to the reference characters S2, S4: 'Reboot M-BRD' and 'INITIALIZE') ***to download the firmware from the serial chip to the programmable part*** (See the whole process of Fig. 2, and see column 8, lines 42-55, 'This process is repeated until the entire firmware upgrade has been burned into the non-volatile memory' [With this paragraph, column 8, lines 42-55, Deegan describes a process that burns the firmware upgrade stored in a device such as RAM 36 or dual port RAM 37 (serial chip) into the non-volatile memory in the mother board (programmable part)]).

As per claim 4: Deegan discloses, "***The method of claim 1, the step of networking comprising utilizing one or more of the Internet, LAN, WAN or mixtures thereof***" (see Fig. 1, reference character no. 51, 'ETHERNET' [Ethernet is known as the most widely-installed local area network technology (LAN)]' see column 6, lines 3-4, 'an internet link as part of the link 51').

As per claim 5:

In light of the specification, page 6, paragraph [0026], it describes an engineer desiring to update a firmware image, and it defines updating firmware in the manner of 'seamless' at an interface server as continuing programming the part without special configuration or communication indicating the newer version:

Deegan discloses, "***The method of claim 1, further comprising updating the firmware image file at the firmware server, wherein subsequent downloads of the firmware image file to a programmable part is seamless to the updated firmware***" from giving the term 'firmware upgrade' where this is transferred to the non-volatile memory (NVM) in the Motherboard 20 from the firmware provider (see column 6, lines 20-28). The transfer is performed initially by a user request (column 6, lines 7-14), then it is upgraded immediately after the initial request (see column 6, lines 5-14); and the process of programming is by entirely burning the firmware upgrade into the non-volatile memory (column 8, lines 42-55, 'This process is repeated until the entire firmware upgrade has been burned into the non-volatile memory'). In this manner, Deegan teaches "seamless", because the firmware upgrade is loaded in the non-volatile memory without requiring a special configuration or a communication indication the newer revision.

As per claim 6: Deegan discloses, "***The method of claim 1, wherein the step of networking comprises utilizing a first interface server local*** (see Fig. 1, referring to: reference character no. 38, 'ETHERNET INTERFACE' [the Ethernet interface is local to the motherboard]) ***to the programmable part*** (see Fig. 1, referring to: reference character no. 24, 'NVM') ***and remote from the firmware server***" (see Fig. 1, referring to: reference character no. 40 [The Ethernet interface 38 is remote from the firmware provider 40]).

As per claim 7: Deegan discloses, "***The method of claim 6, wherein the step of utilizing a first interface server comprises coupling the printed circuit board to a connector of the first interface server*** (see Fig. 1, referring to the connection/wiring between ETHERNET INTERFACE/DAUGTHER BOARD and MOTHER BOARD)".

As per claim 8: Deegan discloses, "***The method of claim 1, wherein the step of networking comprises networking the firmware server*** (see column 3, lines 52-65, referring to: 'network link', See Fig 1, reference character no. 51 'ETHERNET') ***with the printed circuit board***" (See Fig. 1, reference

character no. 'MOTHERBOARD' [motherboard is known as a printed circuit board, and Ethernet is networking]).

As per claim 13: Claim 13 recites claim limitation that has the functionality corresponding to the claim 1. Claim 13 is rejected in the same reason set forth in connecting to the rejection of claim 1.

As per claim 14: Claim 14 recites claim limitation that has the functionality corresponding to the claim 4. Claim 14 is rejected in the same reason set forth in connecting to the rejection of claim 4.

As per claim 15: Claim 15 recites claim limitation that has the functionality corresponding to the claim 5. Claim 15 is rejected in the same reason set forth in connecting to the rejection of claim 5.

As per claim 16: Claim 16 recites claim limitation that has the functionality corresponding to the claim 6. Claim 16 is rejected in the same reason set forth in connecting to the rejection of claim 6.

As per claim 17: Claim 17 recites claim limitation that has the functionality corresponding to the claim 7. Claim 17 is rejected in the same reason set forth in connecting to the rejection of claim 7.

As per claim 18: Deegan discloses, "***The method of claim 16, wherein the step of networking comprises simultaneously networking a plurality of interface servers to the firmware server***" (see column 3, lines 56-61, referring to: 'so that the firmware upgrade can be nearly simultaneously downloaded to the plurality of networked processor modules at once').

As per claim 19: Deegan discloses, ***"The method of claim 16, wherein the step of utilizing the interface servers comprises networking devices*** (see column 3, lines 61-65, referring to: 'having built-in communication ports') ***within one or more of the circuit boards to a network coupled to the firmware server*** (See Fig. 1)".

As per claim 20: Deegan discloses, "***The method of claim 19, further comprising the step of concurrently programming a plurality of programmable parts through downloading, over the network, a plurality of the image files to the plurality of programmable parts***" (see column 3, lines 56-61, referring to: 'so that the firmware upgrade can be nearly simultaneously downloaded to the plurality of networked processor modules at once'). With regards to claim limitation: "***plurality of the image files to the plurality of programmable parts***", Deegan shows a plurality of 'Processor Modules' (Fig. 3, reference character 20', and see column 9, lines 15-21), where these processor modules are connected to a firmware provider (reference character no. 40).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deegan et al., (US no. 6,055,632).

Given the broadest reasonable interpretation of followed claim in light of the specification:

As per claim 9:

Claim 9 recites a system that performs the functionality corresponding the to the method recited by claim 1, where Deegan's teaching covers the limitation of claim 9, "***A system for programming programmable parts in a manufacturing line, comprising:***

a firmware server connected to a network for storing one or more firmware image files (see Fig. 1 referring reference character 40)***;***

one or more interface servers (see Fig. 3 referring reference character 51) ***with the manufacturing line connected to the network,***

for capturing at least one of the image files from the firmware server (see column 3, lines 18-29, referring to: 'transferring a firmware update over a network')***; and one or more printed circuit boards with one or more programmable parts connected with at least one of the interface servers*** (see Fig. 1, reference character 20)***, for programming at least one of the programmable parts with firmware corresponding to at least one of the image files*** (see Fig. 1, reference character no. 51 "ETHERNET"; and see column 3, lines 52-65, referring to 'network link, firmware upgrade can be downloaded into a processor module of a programmable controller system from a firmware provider")".

Deegan does not address ***"with the manufacturing line connected to the network".*** However, Deegan shows the parts which are connected separately (Fig.1) for suggesting an assembly connection in manufactory; and Deegan mentions of resultant transportation delay by waiting a field service personnel (column 2, lines 39-46) for suggesting cost and time consuming without network's supports.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to extend the connections of Deegan's teaching (separated connections) for upgrading firmware process toward an assembly line with the motivation for taking advantage of network downloading and available extensions of separated computer's parts. Doing so would save installation costs and time consuming.

As per claim 10:

Deegan discloses the system as addressed above in accordance to the limitation of claim 9, and further discloses, "***wherein one of the interface server sequentially connects with a plurality of printed circuit boards***" (see Fig 1, DAUGHTER BOARD (Reference character 30) connected to MOTHER BOARD (Reference character 20)).

As per claim 11: Deegan discloses the system as addressed above in accordance to the limitation of claim 10, and further discloses, "***The system of claim 10, the one interface server comprising a connector for physically coupling with the plurality of circuit boards***" (Deegan's discussing a conventional connection: column 1, lines 30-41, 'The processor module includes a connector which is adapted for receiving the programming card'. Deegan's discussing a generic connection: column 5, lines 25-30, 'an appropriate mounting scheme'; Deegan's discussing a plurality of processor modules having a communication port: column 4, lines 49-55, 'processor modules having a communication port disposed on a communication daughter board').

As per claim 12: Deegan discloses the system as addressed above in accordance to the limitation of claim 11, and further discloses, "***The system of claim 11, the connector having one or more pins*** (inherent in a conventional connector of a computer connector port, herein Deegan mentions the connection as "adapted" (column 1, lines 30-41), or "mounting scheme" (column 5, lines 25-30) ***that interface in a programming configuration*** (see column 7, lines 26-36, 'Ethernet interface 38 might be configured automatically or manually') ***with pads or pins on the plurality of printed circuit boards to program the programmable parts***" (see column 4, lines 49-55, 'processor modules having a communication port disposed on a communication daughter board [the plurality of printed circuit boards]').

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Biondi, US No. 6,622,246 B1, discloses a method for writing software into a programmable memory and a method for initiating program control.

Northcutt et al, EP 1 043 656 A2, discloses a method for synchronizing firmware associated with a first computer and a second computer.

Keahey, "Programming of Flash with ICT Rights and Responsibilities", 2000 IEEE, discusses of manifacturies which bring flash programing in-line.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552.

The fax phone numbers:

(703) 872-9306 (for formal communication intended for entry);

(703) 746-5429 (for informal or draft communication, please label "PROPOSED" or "DRAFT").

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TED T. VO

Patent Examiner
Art Unit: 2122
December 24, 2003